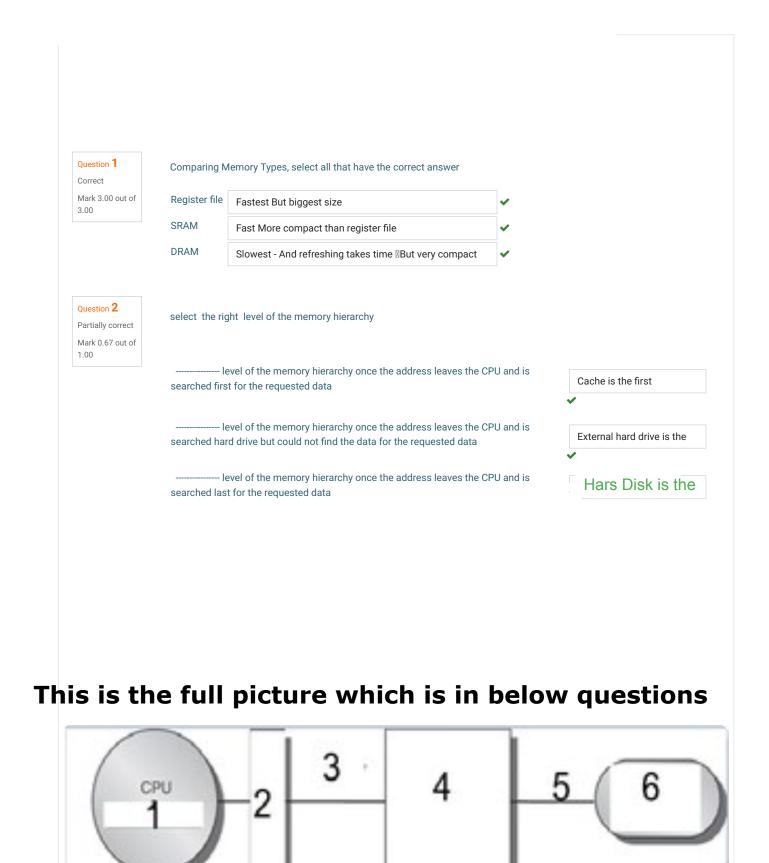
بب التنويه أنه كل الإجابات صحيحة (برأي الدكتور) وموجودات بسلايدات الدكتور خضر محمد



Question **3** Partially correct

Match or write the name of the component to the number. Components are i/o device, registers (D-FF), Main Memory, Fast Memory

Partially correct Mark 2.25 out of 3.00

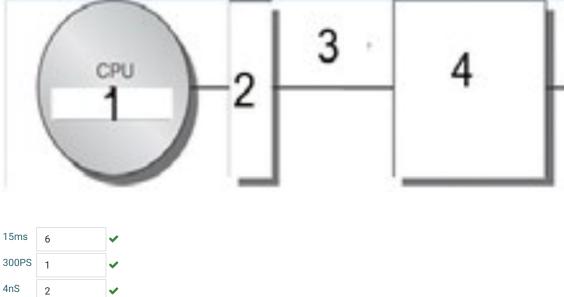
> CPU i/o device 6 reg 1 main memory 4 × 2 is the right answer "Depends on Dr.Khader opinion fast mem 1 Match speed/delay , giving that available values are 120ns, 15ms, 300ps,4ns,

Question **4** Correct Mark 4.00 out of 4.00

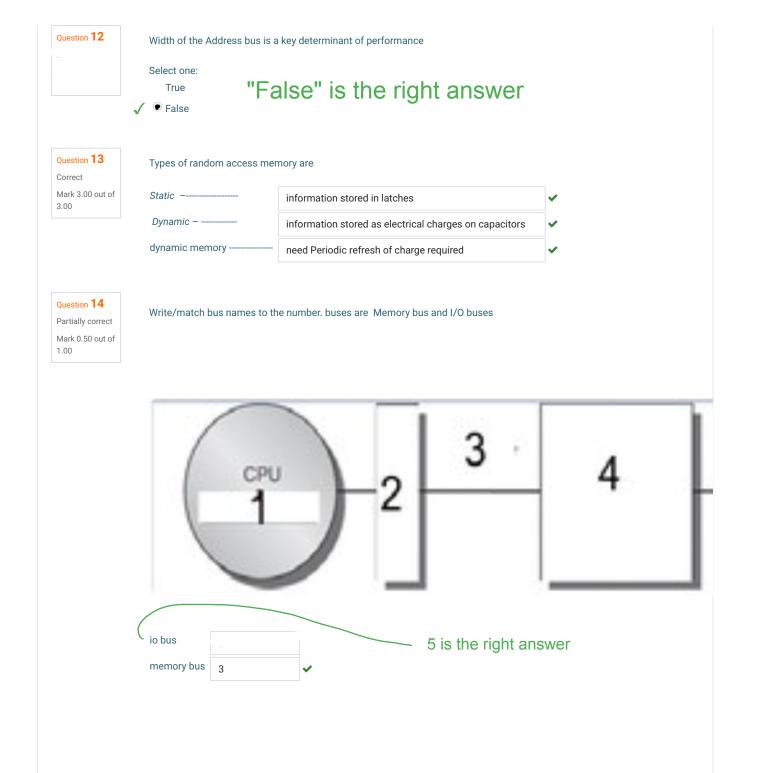
120nS

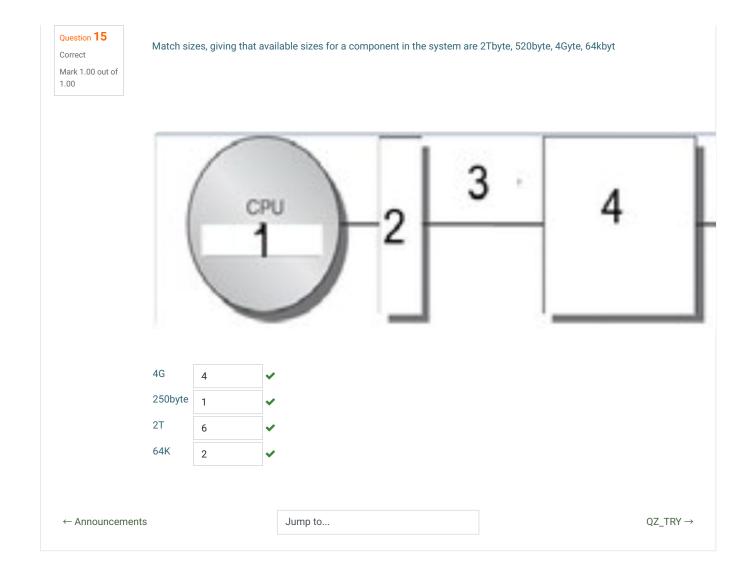
4

~



Question 5 Partially correct		Speeding computers up can be done by (select all that apply)	
		Select one or more:	
		🖉 a. Pipeliningng 🛩	
		b. reduce clock cycle	
		🗹 c. On board L1 & L2 cache 🗸	
Question 6		Miss rate increased if Cache Size (bytes)	
Mark 0.00 out of 1.00		Select one:	
1.00		 a. Will not be affected by size 	
		b. increase	
	~	 ✓ ● c. decrease 	
		d. stay same	
Question 7 Incorrect		There are three main unites to from computers, which are they ?	
1.50	1	Answer: CPU,Memory and Input/Output devices	
Question 8		Data Bus width determines the maximum memory capacity of the system	
Correct		Select one:	
Mark 1.00 out of 1.00		True	
		 ● False ✓ 	
Question 9		if the item is not found in resulting in a page fault, then disk (virtual)	memory) is accessed for it
Correct		In the item is not round in resulting in a page raut, then tisk (virtual)	memory), is accessed for it
Mark 1.00 out of 1.00			
		Answer: Main memory	~
Question 10		General Orgamizatin	
Correct Mark 1.00 out of		checks for interrupt Indicated by an interrupt signal If no interrupt,	
1.00		decode next instruction	The Processor
]		✓
		80286	16 Mbyte memory addressable
			✓
		Increase the hardware speed of the processor can be done Fundamentally by	shrinking logic gate size
		increase the hardware speed of the processor can be done i diruamentally by	✓
Question 11			
		A large enough miss penalty will cause a substantial decrease in CPU to execute when all memory accesses are hits and only data accesses are during loads and	-
ark 0.00 out of		when all memory accesses are hits and only data accesses are during loads and or stores). if miss penalty is 25 clock cycles, and the miss rate is 2%	Stores (50% of all instructions are 1080S
1.00		How much slower because of cache misses? what is the impact on CPI?	





<u>Data retention summary</u> <u>Switch to the standard theme</u>